ACCURATE NONLINEAR TRANSISTOR MODELING USING PULSED S PARAMETERS MEASUREMENTS UNDER PULSED BIAS CONDITIONS

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ABSTRACT

Accurate design of non-linear MICS and MMICS needs accurate modeling of transistors. Two methods are available today, which suffer from several drawbacks:

- In the first method, S parameters are measured at different DC bias points and a small signal model is extracted with elements depending on bias variables. This method ignores temperature effects due to DC dissipation and cannot be applied to high power transistors. Moreover, it does not allow measurements near the breakdown region.

- In the second method, the non-linear current sources are extracted from pulsed measurements, and the linear elements from S parameters. However, this method does not allow accurate extraction of the differential elements (such as gm and gd for a FET), moreover this elements cannot be extracted in the pinched region where the pulsed drain current is zero.

To overpass all the former drawbacks a new method is proposed which has been applied to FETS modeling:

The device is characterized by pulsed S parameters measurements under pulsed bias voltages, in the whole plane of Vgs, Vds, including the breakdown and pinched regions.

The resulting transistor model is accurate for all classes of operation : A, AB, B, C ; the method may be applied to very high power bipolar transistors used in pulsed class C-radars.

I - INTRODUCTION

Accurate design of non-linear MICS and MMICS needs accurate modeling of transistors.

Today, there are two preferred measurement methods to derive nonlinear transistor models, valid for FETS and bipolar transistors.

In the first, S-parameters measurements are performed at various DC bias voltages. Using an optimization program, experimental data are fitted to a small signal model with differential elements. For a FET : gm, gd, Cgs, Cdg are taken as bias dependent variables [1], [2].

However, this method suffers from several drawbacks.

- It ignores the dissipation of the transistor in function of the DC bias points: S parameters are measured at different temperatures depending on the bias conditions.

- On the other hand, differential measurements (S parameters) are made at various DC points Vds_0 and Vgs_0. These DC voltages ignore the trapping effects. So that an inaccuracy is introduced when a voltage-dependent element : X(Vgs, Vds) is supposed to take the same value for a DC variation : Vgs_0, Vds_0, and a dynamical variation Vgs, Vds, around a DC bias point.

- S parameters measurements cannot be made in the breakdown region in function of DC bias, so that the validity of a model deduced from this method cannot be used to simulate hightly nonlinear functions such as class B amplifiers with high input voltages.

Finally, this method cannot be applied to high power bipolar transistors used in pulsed radar applications; dissipation does not allows CW measurements with high DC currents.

The second method generally used, [3], [4], [5], requires S parameters measurements, at a given bias point, to extract the values of the linear elements of the transistor model, and pulsed measurements to evaluate the non-linear voltage-controlled current sources.

For an FET, these sources are :

- The drain current generator Ids = f(Vgs, Vds)
- The gate Schottky diode generator Igs = f(Vgs)
- The gate-drain avalanche generator Ids = f(Vgs, Vds).

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If this later method allows to eliminate the drawbacks of the former, it has inherent limitations :

- Pulsed measurements of the currentsources do not give accurate values of the differential elements (gm, gd) and the resulting model does not allow accurate simulations of low level amplifiers, or intermodulation products in power amplifiers.

- The nonlinear resistive elements are not measured in the pinched region.

- Finally the method necessitates two different measurement systems :
one for S measurements and one for pulsed measurements.

II - THE PROPOSED METHOD : THE PULSED S PARAMETERS MEASUREMENTS UNDER PULSED BIAS CONDITIONS

All the former drawbacks may be overpassed by measuring the scattering parameters under pulsed bias conditions :

The FET is biased at a DC point : Vgs_0, Vds_0. Pulsed gate and drain bias voltages are superimposed to the DC value. A pulse vector network is triggered to perform the S parameters measurements during the bias pulses.

The FET is characterized dynamically in the whole Vgs, Vds plane, including avalanche, reverse, and pinched regions by differential measurements (S parameters) for a given DC bias point.

Detailed measurement procedure :

The whole set-up in shown in the photography and detailed in figure 1. The measurementsystem proceeds as follows :

** A fast rise-time pulse voltage is applied to the gate of the FET under test.*

** The gate-voltage generator triggers the pulse network and a low level drain pulse generator with a time delay which may be up to 50 ns.*

** Both gate and drain DC and pulse bias are applied to the FET, with the pulse microwaves, via the vector network outputs.*

The Wiltron 360-PS 20 pulse network allows measurements of pulse signals as narrow as 20 nanoseconds operating over pulse repetition frequencies of 1 KHz to 1 MHz. The rise time measurement of a D.U.T. is limited by the minimum pulse system width : 20 ns.

The dynamic range is greater thant 90 dB at 1 GHz and 85 dB at 20 GHz for a duty factor of 0.1 and is still greater than 65 dB at a duty factor of 0.01.

Pulse bias duration may vary from 200 ns to 1 ms. Pulse repetition rate may be increased from 600 ns to 1 ms.

Since the Wiltron network may give microwave pulses as short as 20 ns, with variable delay, S parameters may be measured at several points along with the bias pulse.

Data processing

For a choosen DC bias point, a FET is characterized by the pulsed S parameters in the whole Vgs, Vds plane, including the avalanche and pinched region.

A small-signal model having nonlinear differential elements depending on the Vgs and Vds variables, is fitted in the whole Vgs, Vds plane, using standard techniques [2], [3].

Resulting curves for each nonlinear element are then fitted with splines, orthogonal polynomials, or analytical equations (depending on the user) and consistancy of gm and gd variations is verified.

To model accurately a FET for all applications, it is sufficient to perform the measurements at 3 different DC bias points :

- A : $Vgs_0 = 0$, $Vds_0 = 0$: for cold-FET applications

- B : $Ids_0 = \frac{Idss}{3}$, $Vds_0 = \frac{Vbreakdown}{2}$: for class A,

and AB applications

- C : $Vgs_0 = V_p$, $Vds_0 = \frac{Vbreakdown}{2}$: for class B and C applications.

Results obtained :

Figure 2 shows the nonlinear equivalent circuit of a FET. The nonlinear elements of the model are : gm, gd, ga, g_g, Cgs, and Cg_d some of these elements are shown in function of Vds and Vgs in the figures 3, 4, 5, 6.

The results concern a FET DC biased at $Vas_0 = 0^V$, $Vds_0 = 0^V$.

III - CONCLUSION

An improved method for accurate nonlinear modelling of transistors, has been proposed. It allows to overpass the drawbacks of the two methods generally used : It is based on pulse S parameters measurements under pulsed bias conditions. Such procedure takes into account the dynamical variations without varying the temperature of the device under test. The method have been used successfully with FET transistors and may be extended to very high power bipolar transistors used in pulse - class C - radar applications.

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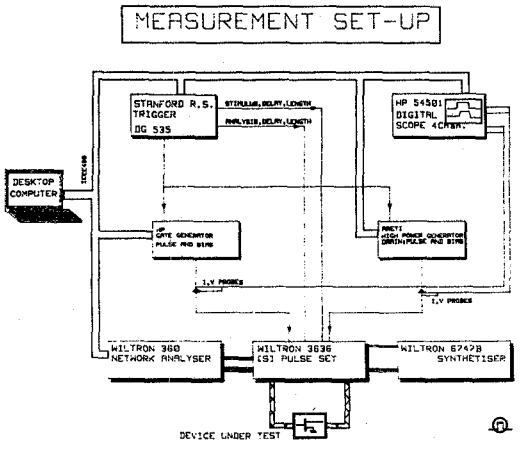
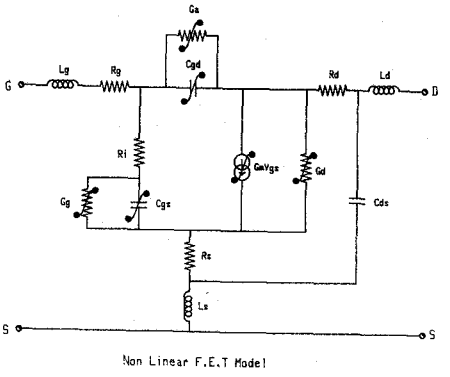
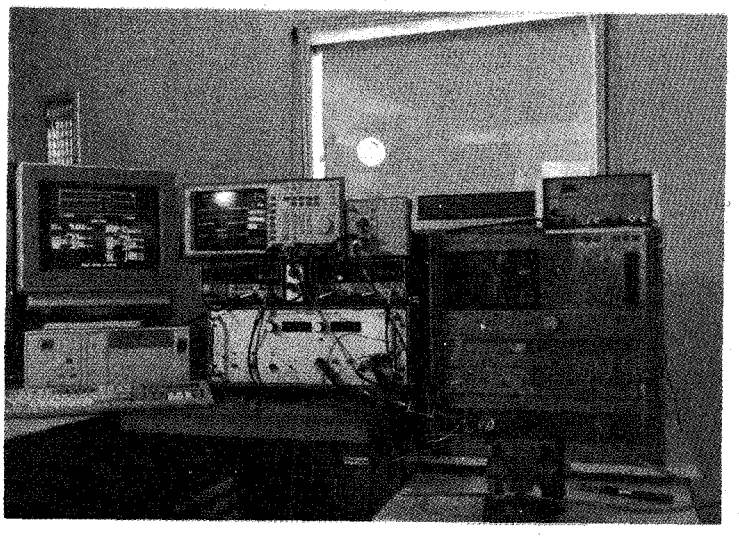


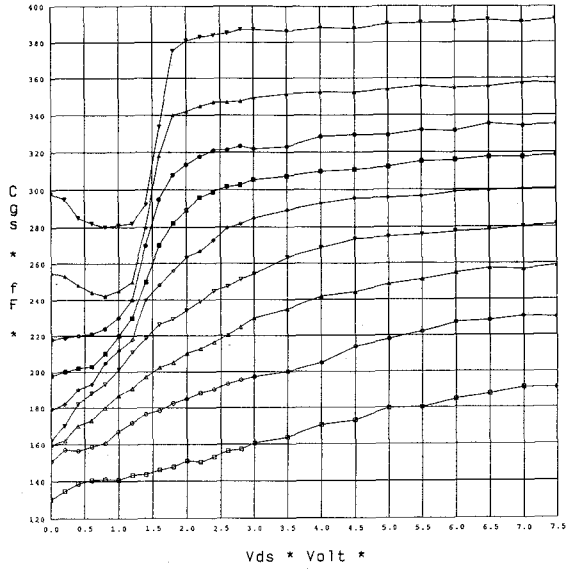
FIG 1

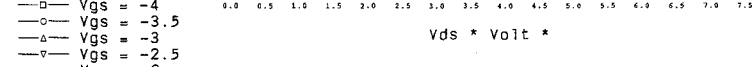


Non Linear F.E.T Model

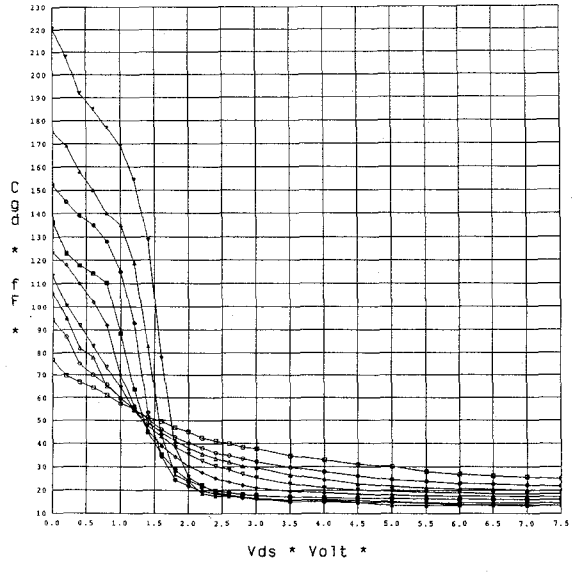


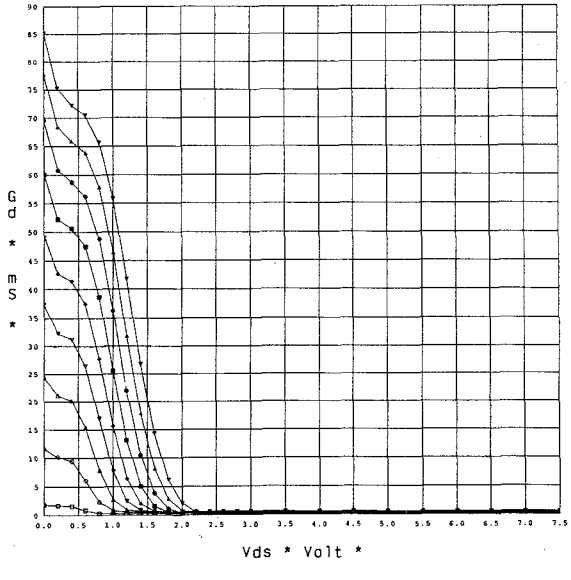
Photography of the measurement-system


Cgs * fF *
Vds * Volt *


Vgs = -4
Vgs = -3.5
Vgs = -3
Vgs = -2.5
Vgs = -2
Vgs = -1.5
Vgs = -1
Vgs = -0.5
Vgs = 0

Gm * mS *
Vds * Volt *


Cgd * fF *
Vds * Volt *


Gds * mS *
Vds * Volt *